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Design and Analysis of Various Full Subtractor Methods to Propose a Customized Design for Enhancing the Performance of a SoC

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Abstract- Advancements in technology have led to an increase in the transistor density on chip which in turn leads to creation of a complete System on Chip (SoC). In addition to which, shifting the focus towards the existing low-level design modifications, leads to further improvement in chip density, resulting in more than one system on a chip, called systems on chip. In this paper, author focuses on the design and analysis of various low level subtractor design modifications and suggests the most feasible design technique. These low level subtractor designs, when used in the top-level hierarchical design of an ALU unit, leads to an enhanced performance of a system which reduces the power, timing and number of transistors occupied on the chip. The various methods of a full subtractor (FS) design have been implemented using Electric tool which utilizes 180nm CMOS technology. After analysing the results obtained from these different methods, using two XOR gates and a 2:1 Multiplexer (MUX) to design a Full Subtractor circuit has proven to be the most feasible design for a full subtractor as it utilizes 44 transistors with a propagation delay of 0.0465 ns and power consumption of 0.117µW which makes it the most optimized design compared to all other methods.

Index Terms- Full subtractor, System on Chip, Power Optimization, Timing Analysis, Efficiency, CMOS Technology, Electric tool.

1. Introduction

Technology has been evolving for many decades, which is compelling the Semiconductor industry to deviate from Moore's law. Such an enhancement in technology leads to a reduction in the transistor size to the lowest nano meter scale, which ultimately increases transistor density on a single die.

As the result of high transistor density, designers are able to accommodate a greater number of functional blocks on a single chip to develop a complete System on Chip (SoC). The feature size of the device is moving towards a lower nano meter scale i.e., less than 7nm, which ultimately meets the energy and power consumption demand of portable battery-operated devices such as laptop, mobile, wrist watches, IoT devices and so forth.

When the transistor length is shrunk below 7 or 4 nm, the second order effects like sub-threshold conduction, hot carrier effects and velocity saturation are observed, that would lead to static power dissipation or a leakage power. To address this issue, the other way of functional block/transistor density can be increased by modifying the original design structure of the combinational or sequential circuits like adder, subtractor, multiplier and counter design in processors or a system. Such modifications allow us to reduce the number of transistors in the basic circuit design. Ultimately the low-level design modification gives a space to develop a multiple system on chip rather than a single system on a chip. Hence there is a research scope to modify the basic digital functional blocks in the future.

In this paper, the authors aim to modify the basic structure of the existing subtractor circuit [1],[2] to obtain maximum efficiency with respect to number of transistors, timing and power consumption using various methods and arriving at a conclusion about the best method among the stated methods.

Organization of this paper is as follows: Section II provides a background on the basic structure of a full subtractor. Section III presents the various other modified full subtractor designs which helps to suggest the best optimized full subtractor design. Section IV shows the comparative result analysis of various design properties of all the full subtractor methods discussed in the paper. Subsequently, section V gives the conclusion of the result.

2. Conventional Method

2.1 Description

A full subtractor is a combinational circuit which performs the subtraction of the three input variables. It is designed using the logic gates AND, NOT, OR and XOR. It has three inputs A, B and C which represent the minuend, subtrahend and the previous borrow. The two outputs D and Bo represent the difference and borrow. Figure 1 represents the logical structure of the conventional Full Subtractor. Based on the Full subtractor truth Table 1 the equations Eq.1 and Eq.2 have been derived.

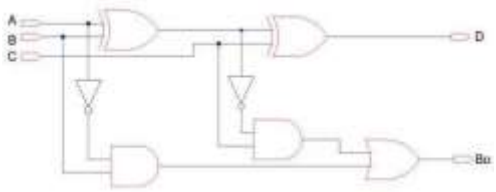

Figure 1: Conventional FS Circuit Diagram

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2.2 Truth Table

Table 1: Conventional FS Truth Table

A	B	C	Difference(D)	Borrow(B)
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

From Table 1 the difference and borrow bits of the output can be obtained as Difference.

$$D = A'B'C + A'BC' + AB'C' + ABC \ldots\ldots\ldots\ldots (1)$$

and Borrow as

$$Br = A'B'C + A'BC' + A'BC + ABC \ldots\ldots\ldots\ldots\ldots (2)$$

Using Karnaugh map the reduced expression for the output bits can be obtained as

$$Br = A \oplus B'C + A'B \ldots\ldots\ldots\ldots (3)$$

This proper choice of a logic strategy is significant because all important constraints governing power dissipation- switching capacitance, transition activity, and short circuit currents are powerfully prejudiced by the chosen logic design constructed on the basis of logic expression using basic gates as shown above.

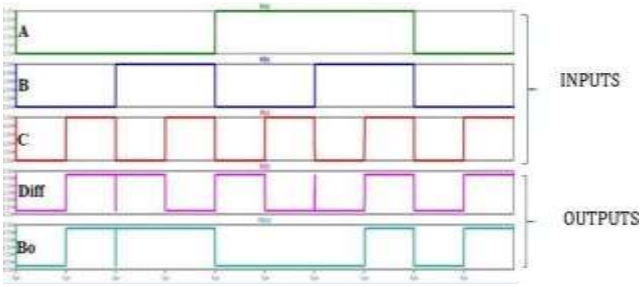

Figure 2: Input and Output waveform of FS

Figure 2 indicates input and output waveform of a conventional FS where A, B and C are the inputs and D and Bo are the outputs.

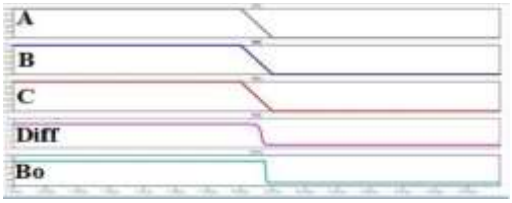

Figure 3: Timing Analysis of Conventional FS

Figure 3 shows the calculation of propagation delay for the conventional method of a full subtractor. This propagation delay is calculated at 50% of the input and 50% of the output. The difference between the input and output helps us to obtain the propagation delay.

Table 2: Shows the Conventional FS Properties

Power(μW)	Number of Transistors	Time(μs)	Propagation Delay(ns)
0.271	46	Tri(Input Rise time)=1.00102 Tro (Output rise time)=1.00144	0.042

Table 2 shows the number of transistors, power and timing analysis of the conventional full subtractor using basic gates. With respect to the timing analysis, the rise time is calculated in order to determine the propagation delay of the circuit.

3. Other modified Full Subtractor Techniques

In this section the authors have tried various other techniques by modifying the conventional FS design.

3.1 Method-1 Using two XOR gates and a 2:1 MUX

3.1.1 Description

In the borrow stage of this method, the AND and OR gates are replaced by a Multiplexer (MUX). For the difference stage, the design of the conventional FS i.e.two XOR gates have been retained, as shown in Figure 4.

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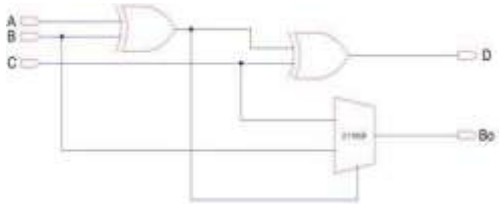

Figure 4: Shows Modified Method-1 FS

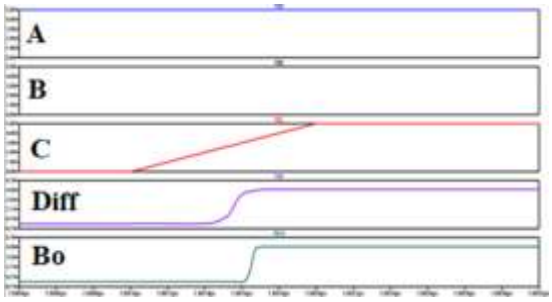

Figure 5: Timing Analysis of Method-1

Figure 5 shows the waveform used for calculation of propagation delay for a full subtractor using 2 XOR gates and 2:1 MUX.

Table 3: Properties of Modified FS Design using method-1

Power(μW)	Number of Transistors	Time(μs)	Propagation Delay(ns)
0.117	44	Tri=7.00100 Tro=7.001465	0.0465

Table 3 shows the result analysis of modified method-1 which shows that the number of transistors and the power have decreased significantly. This implies that method-1 is better than the conventional full subtractor design, with respect to the number of transistors and power utilization for the circuit.

3.2 **Method-2** Using XNOR Gate and two MUX

3.2.1 Description

In this method both difference and borrow stages are modified. The Difference stage is obtained using a 2:1 MUX and logic gates. The borrow stage is realised using a 2:1 MUX is as shown in figure6.

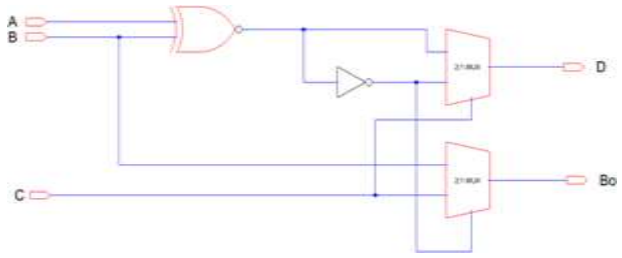

Figure 6: Circuit Diagram of FS using XNOR Gate, NOT Gate and 2:1 MUX

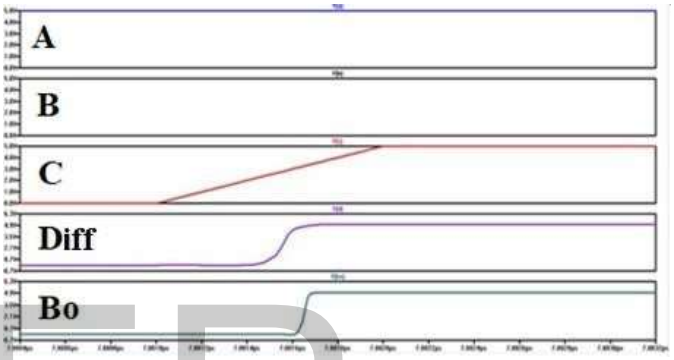

Figure 7: Timing Analysis of Method-2

Figure 7. shows the calculation of propagation delay for a full subtractor using XNOR gates and 2:1 MUX.

Table 4: Properties of FS Design using Method-2

Power(μW)	Number of Transistors	Time(μs)	Propagation Delay(ns)
0.250uW	54	Tri=7.001008 Tro=7.001662	0.0654

Table 4 shows the result analysis of Method 2, after analysis it can be observed that all the parameters have increased. Therefore, this design cannot be considered as one of the optimized methods.

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3.3 Method-3 Using two 4:1 MUX

3.3.1 Description

In this method, both the difference and the borrow stages have been modified to further optimize the design. In method-2, a combination of logic gates and 4:1MUX was used to implement the difference stage, which has been replaced by a 4:1 MUX in this method. To implement the borrow stage, a 4:1 MUX is used. The realization of this design is done using VEM technique as shown in table 5, and figure 8 which shows the logical structure of this method.

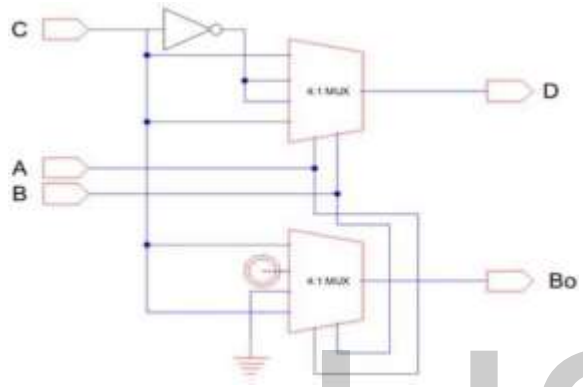

Figure 8: Circuit Diagram for FS using two 4:1 MUX

3.3.2 VEM Table

Table 5: VEM Table for Method-3

A	B	C	D	Bo	Input to multiplexers	
					M1	M2
0	0	0	0	0	C	C
0	0	1	1	1		
0	1	0	1	1	$\bar{C}$	1
0	1	1	0	1		
1	0	0	1	0	$\bar{C}$	0
1	0	1	0	0		
1	1	0	0	0	C	C
1	1	1	1	1		

Variable Entrant Mapping (VEM), is used to increase the effective size of a k-map, thereby allowing a smaller map to handle a larger number of variables. Therefore, VEM is used to realise the output equations required for the method 3. As per table 5, M1 output variable are the inputs for the first MUX and M2 output variables are the inputs for the second MUX, as shown in Figure 8.

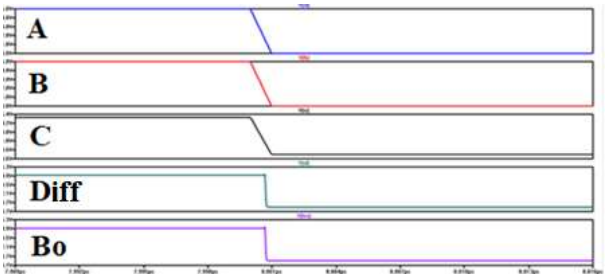

Figure 9: Timing Analysis of Method-3

Figure 9 shows the calculation of propagation delay for a full subtractor using two 4:1 MUXs.

Table 6: Properties of FS Design using Method-3

Power(µW)	Number of Transistors	Time(µs)	Propagation Delay(ns)
0.112uW	122	Tri=7.001004 Tro=7.001716	0.0712

With reference Table 6 we notice that the power consumed by a 4:1 MUX is comparatively lesser than the previous methods. However, the number of transistors significantly increases on using a 4:1 MUX to obtain Difference and Borrow.

4. Result Analysis

Table 7: Comparison Table for all the methods

Parameters	Using Conventional Full Subtractor	Method 1 Using 2 XOR gates and a 2:1 MUX	Method 2 Using 1 XNOR gates and two 2:1 MUX	Method 3 Using two 4:1 multiplexers
Power (uW)	0.271	0.117	0.250	0.112
Propagation delay(ns)	0.042	0.0465	0.0654	0.0712
Number of transistors	46	44	54	122

This section [5] describes the result analysis of various Full Subtractor methods and it is simulated on Electric software using 180nm technology with a supply voltage of 5V. From Comparison Table 7, it can be inferred that the Conventional method has the least propagation delay (0.042 ns) but the power consumed is the most amongst all the methods (0.271 µW). Method 1 is the most optimised design as it utilises a lesser number of transistors (44) compared to other methods thereby significantly reducing the power consumption

(0.117 µW). The following can be inferred about the other methods: Method 2 has the highest amount of power consumed (0.250 µW). The propagation delay (0.0654 ns) and number of transistors used (54) are higher than that of the conventional method and method 1. Method 3 utilizes the greatest number of transistors (122) and has a higher propagation delay (0.0712 ns) compared to all other methods therefore making it much slower and less efficient. However, the power consumed (0.112 µW) is the least in this method as it uses two 4:1 MUX. Figure 10 shows the graphical representation of comparative analysis of all the method with respect to number of transistors, power consumption, and the propagation delay

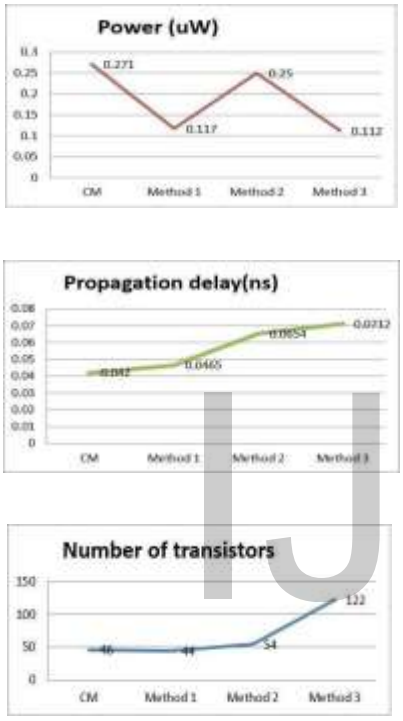

Figure 10: Shows the Graphical Comparison Analysis of all methods

5. Conclusion

Due to advancements in technology, the need for minimum power consumption, minimum transistor count and less propagation delay has driven the need for optimized low-level designs to further enhance the density of the SoC design. This research work proposes various full subtractor designs and analyses the various design parameters to suggest the best method. From the analysis, it can be inferred that using two XOR gates and a 2:1 MUX in the modified FS leads to lower power consumption due to a smaller number of transistors used in this method compared to all other methods. Hence, it can be concluded that using two XOR gates and a 2:1 MUX is the most optimized way to design a FS, which can be incorporated in the ALU of a system. The suggested design also makes it possible for the system to be portable and be applied in energy efficient applications.

References

[1] Padmaja, M., & Anusha, S. Design of Ripple Borrow Subtractor using different logic techniques. In International Journal of Engineering Research and Applications ISSN : 2248-9622, Vol. 3, Issue 5, Sep-Oct 2013, pp.1979-1983
[2] M.Mahaboob Basha,K.Venkata Ramanaiah,P. Ramana Reddy,"Design of Near Threshold 10T- Full Subtractor Circuit for Energy Efficient Signal Processing Application",I.J. Image, Graphics and Signal Processing, 2017, 12, 23-29
[3] Sreelatha, P., Lakshmi, P. K., & Rao, R. (2017, May). Performance analysis of 1-bit full adder using different design techniques. In 2017 2nd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology *(RTEICT)* (pp. 2262-2266). IEEE.
[4] Padmaja, M., & Anusha, S. Design of Ripple Borrow Subtractor using different logic techniques. In International Journal of Engineering Research and Applications ISSN : 2248-9622, Vol. 3, Issue 5, Sep-Oct 2013, pp.1979-1983
[5] Manpreet Kaur,Amandeep Kaur "Review Paper on Vedic Multiplier by Using Different Methods" International Journal of Engineering Development and Research (IJEDR) Volume 6, Issue 2(June 2018).
[6] U.Palani1, G. Amuthavalli, R. Gunasundari "Power-Efficient 32 Bit Adder-Subtractor with Integrated Logic Design and Leakage Mitigation" International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249-8958, Volume-8 Issue-5, June 2019
[7] Padmanabhan Balasubramanian, Nikos E. Mastorakis "High Speed Gate Level Synchronous Full Adder Designs" WSEAS TRANSACTIONS on CIRCUITS and SYSTEMS
[8] C.Senthilpari Member IEEE, K.Diwakar, C.M.R.Prabhu Member IEEE,Ajay Kumar Singh Member IEEE "Power Deduction in Digital Signal Processing Circuit using Inventive CPL Subtractor Circuit" ICSE2006 Proc. 2006, Kuala Lumpur, Malaysia
[9] Sugandha Gaur, Abhilasha "Control Signal Based Full Adder/Subtractor" International Journal of Scientific & Engineering Research, Volume 7, Issue 10, October-2016 ISSN 2229-5518
[10] Parminder Kaur & Balwinder singh Dhaliwal," Design of Fault Tolerant Full Adder/Subtarctor Using Reversible Gates" International Conference on Computer Communication and Informatics (ICCCI) -2012.
[11] Prashanth. N. G, Havyas. V. B, Prashantha. N. C,
Naveena Pai G4, Dinesha Shetty G," Design of Efficient Reversible Fault Tolerant Carry Skip Adder/Subtractor"International Journal of Emerging Technology and Advanced Engineering, Volume 3, Issue 11, November 2013.
[12] Ankur Sarker, Avishek Bose, Shalini Gupta," Design of a Compact Fault Tolerant Adder/Subtractor Circuits Using Parity Preserving Reversible Gates ", 17th Int'l Conf. on Computer and Information Technology, 22-23 December 2014.
[13] Dondapati Naresh, V.B.Gopala Krishna,"Design and
Implementation of Fault Tolerant Carry Skip Adder or Subtractor using Reversible Logic Gates", ISSN 2322-0929 Vol.02, Issue.07, October-2014.
[14] S.Mounika, Dr.M.Gurunandabaabu," A Novel Design for carry skip adder using purity preserving reversible logic gates", International Journal & Magazine of Engineering, Technology, Management and Research, Volume No: (2015).
[15] Subramanian Saravanan1, Ila Vennila, Sudha Mohanram,"
Design and Implementation of an Efficient Reversible Comparator Using TR Gate, "Circuits and Systems, 2016".